AMENDMENTS TO CLAIMS

• Please amend claims 1-10 and cancel claims 11-20 as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A method of manufacturing an integrated circuit comprising:

~~depositing~~ forming a charge-trapping dielectric layer over a semiconductor substrate;

forming first and second bitlines in the semiconductor substrate;

forming a wordline over the charge-trapping dielectric layer; and

~~depositing~~ forming a dielectric layer over the wordline wherein ~~a~~ for a structure selected from ~~a group consisting~~ at least one of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof~~.~~, the structure contains deuterium diffused from another structure selected from at least one of the charge-trapping dielectric layer, the wordline, the dielectric layer, and a combination thereof.

2. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 1 wherein the ~~depositing and~~ forming includes ~~depositing~~ forming deuterated materials for a structure selected from ~~a group consisting~~ at least one of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof.

3. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 1 including deuterating a structure selected from ~~a group consisting~~ at least one of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof.

4. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 1 wherein ~~depositing~~ the forming the charge-trapping layer, the wordline, and the interlayer dielectric layer deposits materials selected from ~~a group consisting~~ at least one of a deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a polysilicon, a glass, and a combination thereof.

5. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 1 wherein the ~~depositing and~~ forming the charge-trapping layer, the wordline, and the interlayer dielectric layer uses ~~use~~ a process selected from ~~a group consisting~~ at least one of high-density plasma deposition, rapid thermal chemical vapor deposition, low pressure chemical vapor deposition, rapid thermal oxidation, annealing in deuterium gas, and a combination thereof.

6. (currently amended) A method of manufacturing an integrated circuit comprising:

~~depositing~~ forming a first dielectric layer on a semiconductor substrate;

~~depositing~~ forming a charge-trapping layer over the first dielectric layer;

~~depositing~~ forming a second dielectric layer over the charge-trapping layer;

forming first and second bitlines in the semiconductor substrate;

forming a wordline over the second dielectric layer;

forming a spacer around the wordline; and

~~depositing~~ forming an interlayer dielectric layer over the wordline wherein for a structure selected from ~~a group consisting~~ at least one of the first dielectric layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof is deuterated, the structure contains deuterium diffused from another structure selected from at least one of the first dielectric layers, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and the combination thereof.

7. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 6 wherein the ~~depositing and~~ forming ~~include depositing~~ includes forming deuterated materials for a structure selected from ~~a group consisting~~ at least one of the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof.

8. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 6 including deuterating a structure selected from ~~a group consisting~~ at least one of the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof.

9. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 6 wherein ~~depositing~~ the forming the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, and the interlayer dielectric layer deposits materials selected from ~~a group consisting~~ at least one of deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a polysilicon, a glass, and a combination thereof.

10. (currently amended) The method of manufacturing an integrated circuit as claimed in claim 1 wherein the ~~depositing and~~ forming the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, and the interlayer dielectric layer uses ~~use~~ a process selected from ~~a group consisting~~ at least one of high-density plasma deposition, rapid thermal chemical vapor deposition, low pressure chemical vapor deposition, rapid thermal oxidation, annealing in deuterium gas, and a combination thereof.

11-20 (cancelled)